A REVIEW ON FPGA IMPLEMENTATION OF POLYPHASE FILTER

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***Abstract*— Use of Digital filters are in digital transmitter / receiver side. One access to parallel digital signal processing splits a high bandwidth signal into multiple lower bandwidth (rate) signals by an analysis bank. After processing by using synthesis bank, the subband signals are recombined into a fullband output signal. This paper describes a polyphase filter bank and implementation on FPGA-based architectures according to size, timing and bandwidth requirements. In this paper we study implementation of a Vedic Multiplier based polyphase filter which will be faster and more accurate than the existing systems.Using the polyphase FIR filter to filter out signal frequencies which are not needed.**

Keywords - FIR filters; FPGA;VHDL;Xilinx;Matlab

I. INTRODUCTION

In the previous study of filter banks and subband processing as well as multi-resolution analysis (MRA) wavelet transforms has occurred at a fast pace. In particular, subband processing of signals is now common in a number of applications such as video encoders/decoders,image,audio; spread spectrum communications systems and acoustic echo cancelers used in hands-free teleconferencing systems. In addition, emerging applications include multiple target tracking in radar. As compared to equivalent fullband processing, subband signal processing often leads to a increase in performance due to the MRA and a reduction in computation due to the lower sampling rate of the subband (component) signals. Also its application is in parallel digital signal processing architectures.

Digital filters forms crucial blocks of digital transmitter and receiver. In digital communication polyphase FIR filters can be used for sample rate conversion as decimation or interpolation filters. The current portion of the collaboration has involved the implementation of a Polyphase Filter bank using hardware architectures and various FPGAs and

Proposed polyphase structure can be very easily incorporated to symbol synchronization subsystem of SDR. The aim is to develop efficient FIR filter structures in VHDL language for RTL synthesis on FPGA. The proposed structures based on distributed arithmetic contain polyphase decimation and interpolation FIR filter models. Main design benefits are: optional logic resources utilization, easy portability using standard HDL libraries and also very good registered performance.

II. LITERATURE REVIEW

L. C. Loong and N. C. Kyun presents the multirate filters design using SDR concept. Two SDR models are considered; one with System Generator and one which was based on Matlab Simulink. The results show that both models can produce the desired audio sample rate. Using SDR concept, processing can be done at any sampling rate, within a wide range of rates. International Journal of Engineering and Technology, Vol. 5, No. 2, 2008.

Prasit Kumar Bandyopadhyay And Arindam Biswas discuss the implementation of FIR Bandpass Filters on FPGAs which will eliminate high frequency noise from audio speech signal. This paper describes about the Noise Extraction system that is designed in Xilinx System. They provide excellent high frequency noise reduction. Journal of Electron Devices, Vol. 17, 2013

Rajesh Mehra And Rashmi Arora gives design and implementation of high speed CIC decimator for wireless applications like GSM. The fully pipelined CIC decimator is designed with Matlab, simulated with Xilinx AccelDSP, synthesized with Xilinx Synthesis Tool (XST), and implemented on Virtex-II based XC2VP50-6 target FPGA device. It reduces the need for expensive antialiasing analog filters. It provides enhanced performance in terms of speed and area utilization. International Journal of Advanced Computer Science and Applications, Vol. 2, No. 5, 2011.

Yonghao Wang and Joshua Reiss present the results of a comparison of different decimation architectures for high resolution sigma delta analogue to digital conversion in terms of passband, transition band performance, simulated signal to noise ratio, and computational cost. They provide excellent comparison of the different multirate filters for low group delay audio applications. Audio Engineering Society Convention Paper 8648 Presented at the 132nd Convention 2012 April.

Rajesh Mehra And Shaily Verma described Interpolator has been designed and simulated by using Direct Form Polyphase Serial and Parallel structures to reduce area and to enhance speed. The result shows that serial interpolator can enhance speed by 5.6% as compared to MAC based design. International Journal of Electrical Electronics &Telecommun ication Engineering, 2013.

Fredric J. Harris and Michael Rice describes the use of a polyphase filter bank to perform the interpolations required for symbol timing synchronization in a sampled data receiver. Separate interpolating filter following the matched filter is not required. IEEE Journal vol. 19, no. 12, December 2001.

III. METHODE USED

We will be using the polyphase FIR filter to filter out signal frequencies which are not needed. In our system we will be implementing a Vedic Multiplier based polyphase filter which will be faster and more accurate than the existing systems.

A. The Vedic Multiplier

The Vedic multiplier is based on the Vedic multiplication formulae (Sutras). For the multiplication of two numbers in the decimal number system these Sutras have been traditionally used. The multiplier is independent of the clock frequency of the processor, their sums and partial products are calculated in parallel. Thus the multiplier is independent of the clock frequency because it needs the same amount of time to calculate the product. To operate at increasingly high clock frequencies, advantage is that it reduces the need of microprocessors. Since it has a quite a regular structure, the processing power of multiplier can easily be increased by increasing the input and output data bus widths. Due to its regular structure property , it can be easily layout in a silicon chip. The Multiplier has benefits that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Thus it is space, time and power efficient.

B. Filter Bank

In signal processing, a **filter bank** separates the input signal into multiple components. A graphic equalizer is one application of a filter bank which can attenuate the components differently and recombine them into a modified version of the original signal. The process of decomposition performed by the filter bank is called *analysis* (meaning analysis of the signal in terms of its components in each sub-band); the output of analysis is referred to as a subband signal with as many subbands as there are filters in the filter bank. The reconstruction process is called *synthesis*, meaning reconstitution of a complete signal resulting from the filtering process.

C. FIR Filter

In signal processing, a **finite impulse response** filter is a filter whose impulse response (or response to any finite length input) is of finite duration, because in finite time it settles to zero. For a causal discrete-time FIR filter of order *N*, each value of the output sequence is a weighted sum of the most recent input values**:**

$$y[n] = b_0 x[n] + b_1 x[n-1] + \cdots + b_N x[n-N]$$

$$= \sum_{i=0}^{N} b_i \cdot x[n-i],$$

where**:**

- $x[n]$ is the input signal,
- $y[n]$ is the output signal,
- N is the filter order; an Nth order filter has $(N+1)$ terms on the right-hand side
- b_i is the value of the impulse response at the *i*'th instant for $0 \leq i \leq N$ of an Nth-order FIR filter. If the filter is a direct form FIR filter then b_i is also a coefficient of the filter .

This computation is known as discrete convolution.

D. Polyphase Filter

The Polyphase filter (PPF) has two important uses. First is that the PPF serves as a bandpass filter. Second is the PPF suppresses the drawbacks of the application of a discrete Fourier transformation (DFT) to data. These drawbacks are DFT leakage and DFT scalloping loss. In signal processing terms the PPF is a linear filter applied on N frequency channels. There are two types of linear filters, which differ in their behavior (response). The First called FIR (Finite Impulse Response) filters. As the name ,the response of these filters to

a single pulse in the input data is finite in time. The second called IIR filters, IIR is Infinite Impulse Response. These filter use their own output from previous calculations performed on a past samples to produce the current output which is formed from the latest sample. This property means that the response of these filters to a single pulse is infinite in time. An explanation of the respective behaviors of filter is shown in Figure 1.

For our implementation of the PPF we have chosen the FIR filter, as they are stable. The stability of the FIR filter comes from their limited response in time. If there are some critical errors in our data, by using a FIR filter only part of our filtered data gets corrupted, this is opposite to IIR filter where all data after the error are affected. The FIR filter is also more easily parallelized since input to each filter is independent of any previous results of that filter.

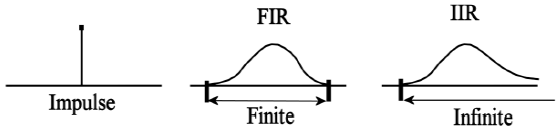


Figure 1. This Figure shows the behaviors of both types of linear Filters to a single pulse (left fig.). The FIR Filter's (middle fig.) response is Finite in time, while the IIR Filter's (right fig.) response is in Finite in time.

E. FPGA

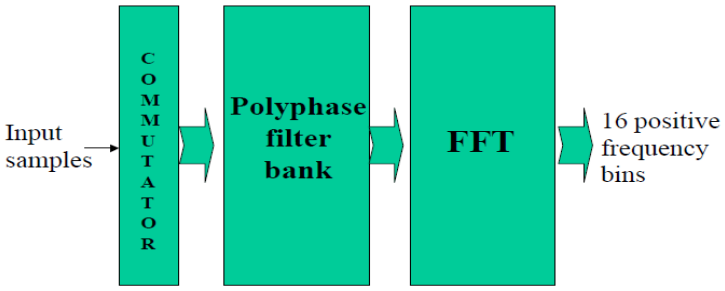
A **field-programmable gate array** (**FPGA**) is an integrated circuit. It is designed to be configured by a customer or a designer after manufacturing – hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL), also used for an application-specific integrated circuit (ASIC).

FPGAs contain an array of programmable logic blocks, and interconnects hierarchy of reconfigurable that allow the blocks to be "wired together", similar to many logic gates that can be inter-wired in different configurations. Logic blocks can be configured to perform complex combinational functions, or simple logic gates like AND and XOR. In most FPGAs, logic blocks also include memory elements, which may be simple flip-flops.

F. Implementation using FPGAs

The polyphase, uniform- filter bank is implemented on a pair of FPGAs. One FPGA for the analysis bank and another for the synthesis bank. In the implementation filterbank, all components of the filter bank are configured in Very high speed integrated circuit Hardware Description Language (VHDL) because of the flexibility of VHDL. This flexibility can be used for purposes of adding more subbands/processors, increasing wordsizes, and/or using sharper analysis/synthesis filters. For instant, changing the number of subbands or the wordsize is easily done in the description by altering a few constants in the source file. A filter bank having four, eight, and sixteen subbands has been described in VHDL and simulated. In addition, the four subband filter bank has been implemented, tested, and verified on FPGAs.

IV. Architecture of Polyphase Filter



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Commutator:
- it distributes signal to n lines
- it reduces clock speed by factor of n

Polyphase Filter bank:
- 32 1-input, 1-output polyphase filters or
- 16 1-input, 2-output optimized polyphase filters

FFT:
- 2n-point real FFT
- n-point complex FFT

V. Fully parallel signed Disributed Arithmetic (DA) FIR model

The structure of VHDL implementation of the proposed fully parallel pipelined FIR filter based on DA is shown in Fig. 2. This type of filter calculates output in a single clock cycle and consists of two main entities: *fir_filter* and *case4x**n***. Entity *fir_filter* is the main part of this model and represents a template, which is only slightly modified for different coefficient filter sets. Input sample vector (*std_logic_vector*) is saved to buffer with length, which is equal to the number of FIR filter taps. This vector is converted to VHDL signed data type. Every clock cycle is new vector obtained and older vectors are shifted. This block has basically shift register function. Then mapping $f(c[n]\times x[n])$ is performed using instance (or instances) of *case4x**n*** entity, where ***n*** is directly

proportional to FIR filter length. For fully parallel operation we need to create ***k*** instances, this means that for every bit of input word one *case4x**n*** instance is required. This is explained with examples in Fig.2 (bottom corner). Entity *case4x**n*** is automatically generated from Matlab (described later). *Pipeline_0* section performs initial calculation of sum of products. This pipeline section can be very comprehensive and for that reason is also automatically generated. Appropriate VHDL code with signal definitions is then placed to *fir_filter* main entity. *Pipeline_1* provides shift-adder operation, embedded multipliers are not utilized. *Pipeline_2* with *FIR_Final stage* form last stage in proposed fully pipelined FIR filter model.

VI. Conclusion

In this paper we are going to implement vedic multiplier based polyphase filter which will be faster and more accurate than the existing systems. By using the polyphase FIR filter to filter out signal frequencies which are not needed. This use for high speed data communication and receiver side filtering in 3G and 4G network.

VII. References

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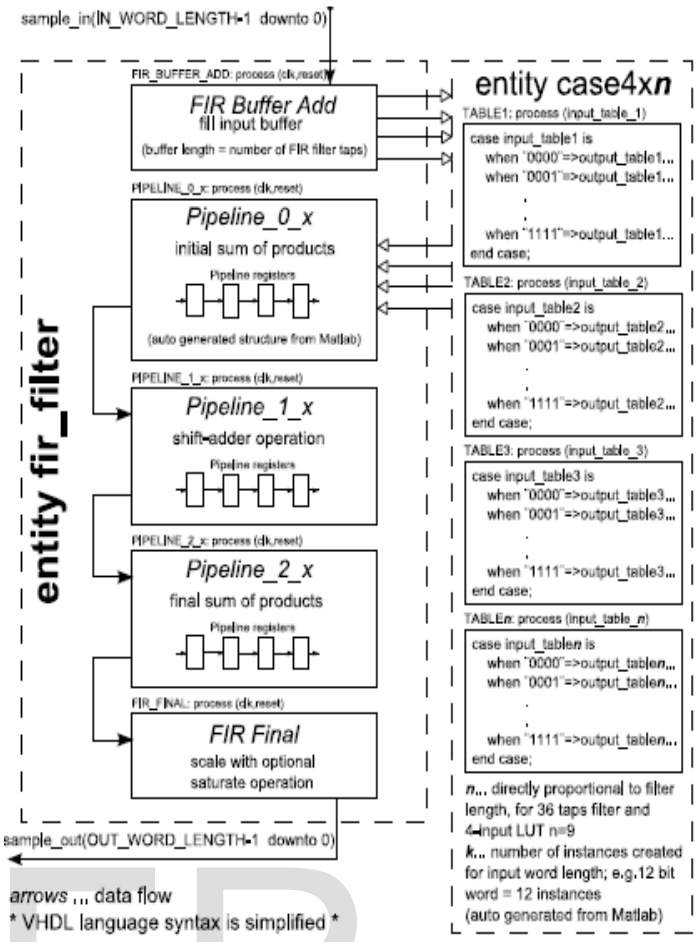

Figure 2. Fully parallel signed DA FIR filter structure

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